



N-Channel 2.5-V (G-S) Battery Switch, ESD Protection

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
28	0.033 @ $V_{GS} = 4.5$ V	4.6
	0.038 @ $V_{GS} = 3.0$ V	4.3
	0.042 @ $V_{GS} = 2.5$ V	4.1



FEATURES

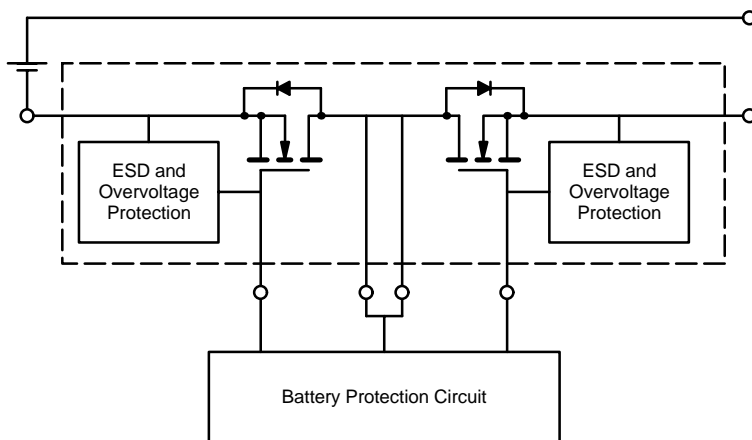
- Low $r_{DS(on)}$
- V_{GS} Max Rating: 14 V
- Exceeds 2-kV ESD Protection
- 28-V V_{DS} Rated
- Symmetrical Voltage Blocking (Off Voltage)

DESCRIPTION

The Si6924AEDQ is a dual n-channel MOSFET with ESD protection and gate over-voltage protection circuitry incorporated into the MOSFET. The device is designed for use in Lithium Ion battery pack circuits. The common-drain construction takes advantage of the typical battery pack topology, allowing a further reduction of the device's on-resistance. The 2-stage input protection circuit is a unique design, consisting of two stages of back-to-back zener diodes separated by a resistor. The first stage diode is designed to absorb most of the ESD energy. The second stage diode is

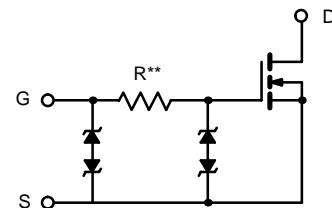
designed to protect the gate from any remaining ESD energy and over-voltages above the gates inherent safe operating range. The series resistor used to limit the current through the second stage diode during over voltage conditions has a maximum value which limits the input current to ≤ 10 mA @ 14 V and the maximum t_{off} to 12 μ s. The Si6924AEDQ has been optimized as a battery or load switch in Lithium Ion applications with the advantage of both a 2.5-V $r_{DS(on)}$ rating and a safe 14-V gate-to-source maximum rating.

APPLICATION CIRCUITS



*Thermal connection to drain pins is required to achieve specific performance.

FIGURE 1. Typical Use In a Lithium Ion Battery Pack

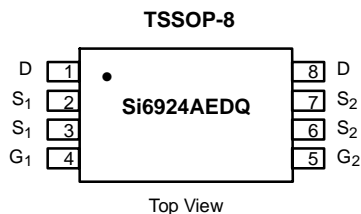


**R typical value is 3.3 k Ω by design.

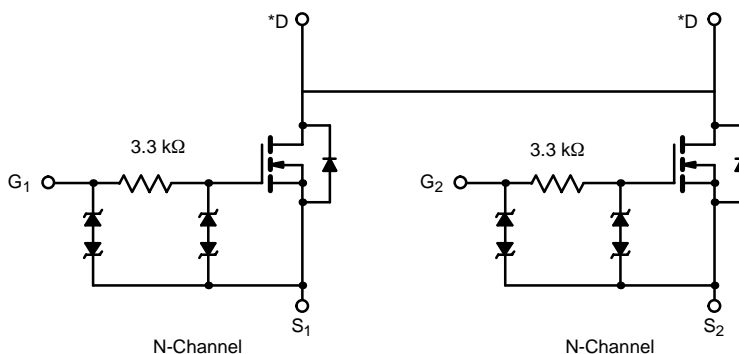
See Typical Characteristics, Gate-Current vs. Gate-Source Voltage, Page 3.

FIGURE 2. Input ESD and Overvoltage Protection Circuit.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Ordering Information: Si6924AEDQ-T1



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FIGURE 3.

FIGURE 4.

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	10 sec	Steady State	Unit
Drain-Source Voltage, Source-Drain Voltage		V _{DS}	28		V
Gate-Source Voltage		V _{GS}	± 14		
Continuous Drain-to-Source Current (T _J = 150°C) ^a	T _A = 25 °C	I _D	4.6	4.1	A
	T _A = 70 °C		3.7	3.2	
Pulsed Drain-to-Source Current		I _{DM}	20		
Pulsed Source Current (Diode Conduction) ^a		I _S	1.2	0.9	
Maximum Power Dissipation ^a	T _A = 25 °C	P _D	1.3	1.0	W
	T _A = 70 °C		0.84	0.64	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	t ≤ 10 sec	R _{thJA}	71	95	°C/W
	Steady State		96	125	
Maximum Junction-to-Foot (Drain)		Steady State	R _{thJF}	56	70

Notes

a. Surface Mounted on FR4 Board.

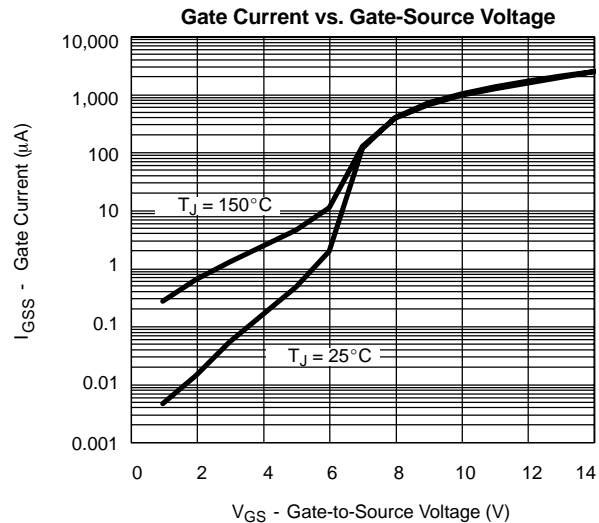
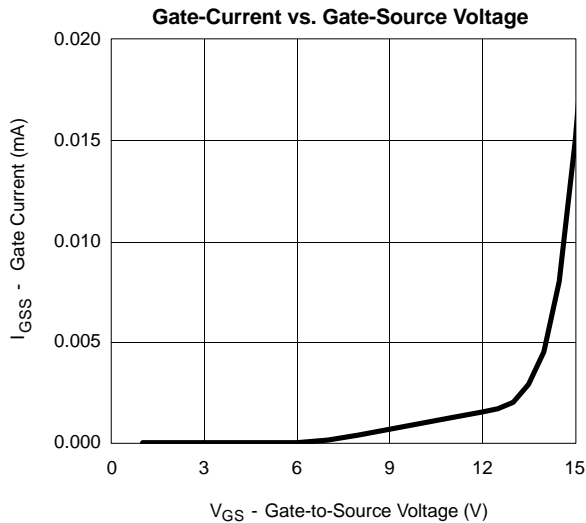


SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.6		1.5	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±4.5 V			±1	μA
		V _{DS} = 0 V, V _{GS} = ±14 V			±20	mA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 22.4 V, V _{GS} = 0 V			1	μA
		V _{DS} = 22.4 V, V _{GS} = 0 V, T _J = 55 °C			5	μA
On-State Drain Current ^b	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 5 V	10			A
Drain-Source On-State Resistance ^b	r _{DS(on)}	V _{GS} = 4.5 V, I _D = 4.6 A		0.022	0.033	Ω
		V _{GS} = 3.0 V, I _D = 4.3 A		0.025	0.038	
		V _{GS} = 2.5 V, I _D = 4.1 A		0.029	0.042	
Forward Transconductance ^b	g _{fs}	V _{DS} = 10 V, I _D = 4.6 A		25		S
Diode Forward Voltage ^b	V _{SD}	I _S = 1.2 A, V _{GS} = 0 V		0.7	1.1	V
Dynamic^a						
Total Gate Charge	Q _g	V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 4.6 A		6.5	10	nC
Gate-Source Charge	Q _{gs}			1.2		
Gate-Drain Charge	Q _{gd}			1.5		
Turn-On Delay Time	t _{d(on)}	V _{DD} = 10 V, R _L = 10 Ω I _D ≅ 1 A, V _{GEN} = 4.5 V, R _G = 6 Ω		0.95	1.5	μs
Rise Time	t _r			1.4	2.1	
Turn-Off Delay Time	t _{d(off)}			7	11	
Fall Time	t _f			3.1	5	

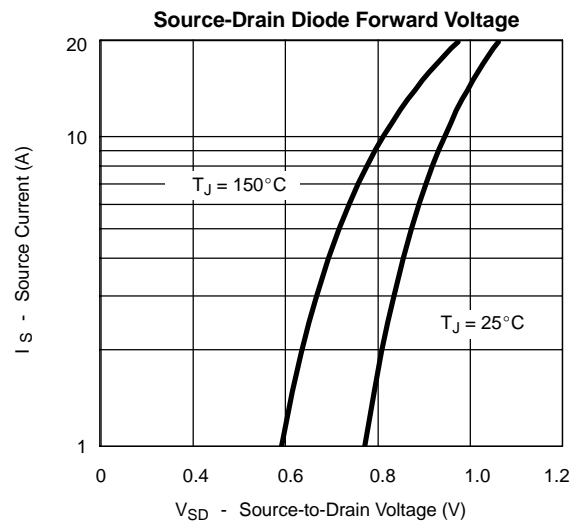
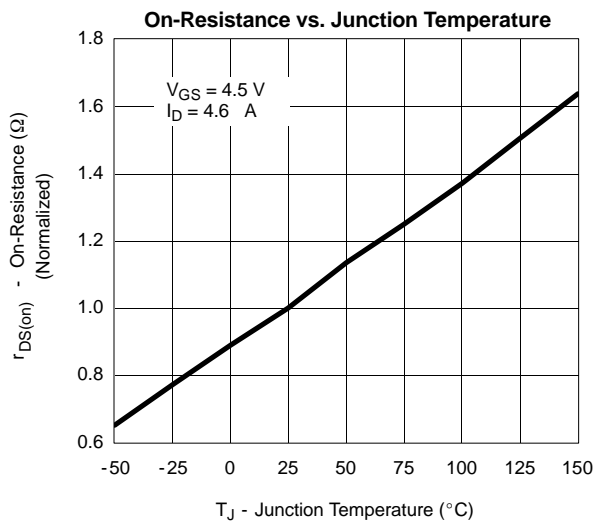
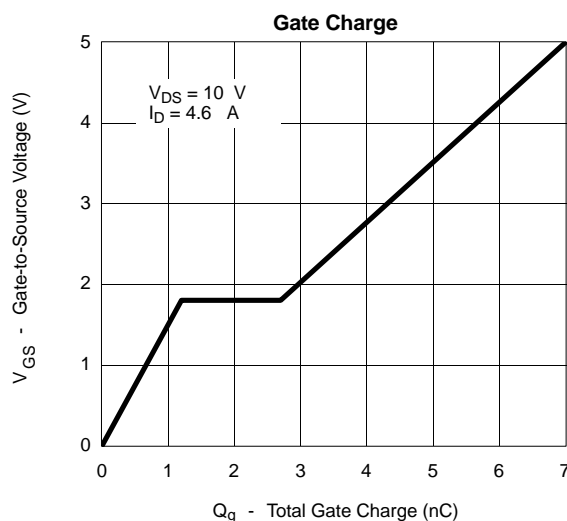
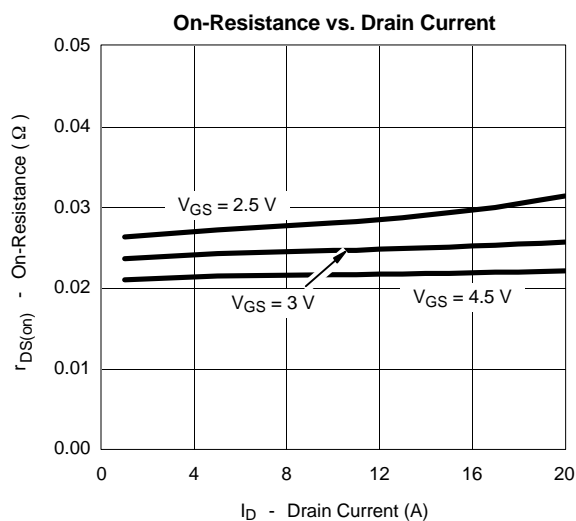
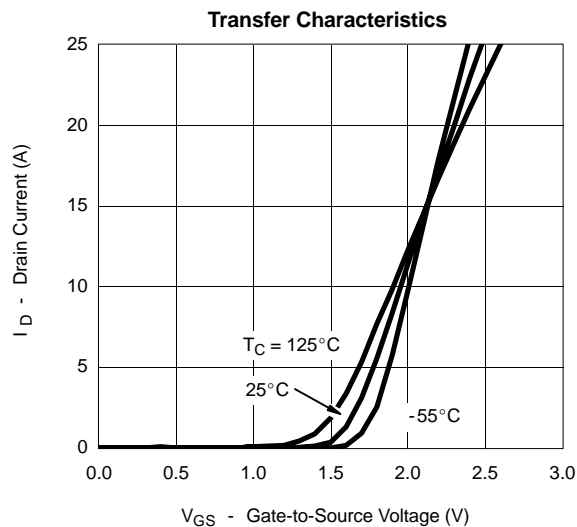
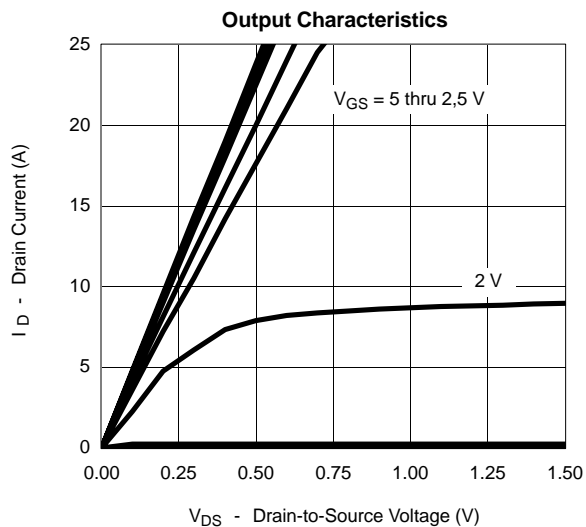
Notes

- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

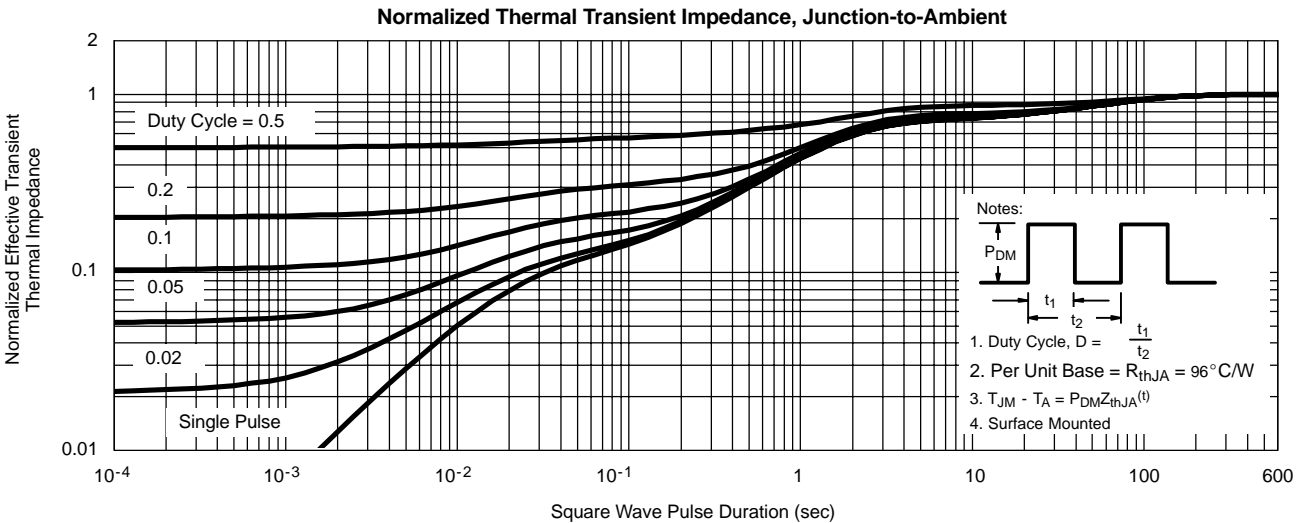
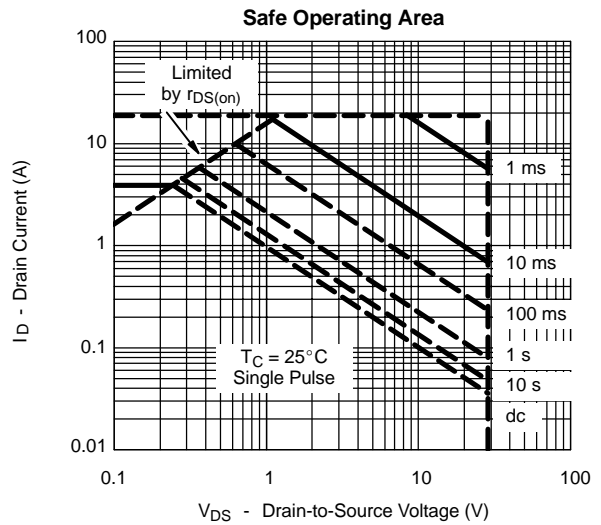
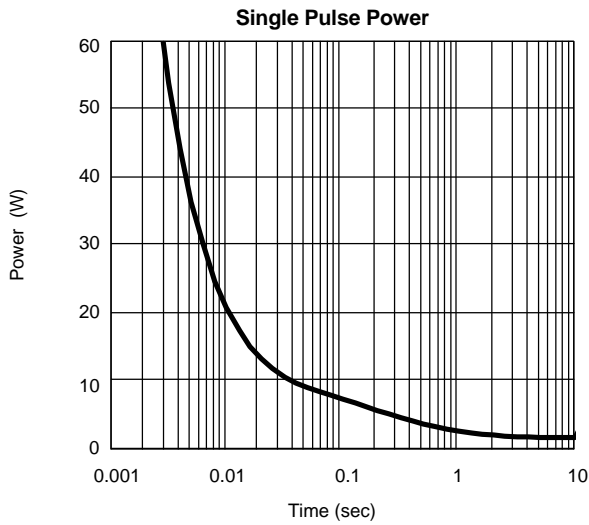
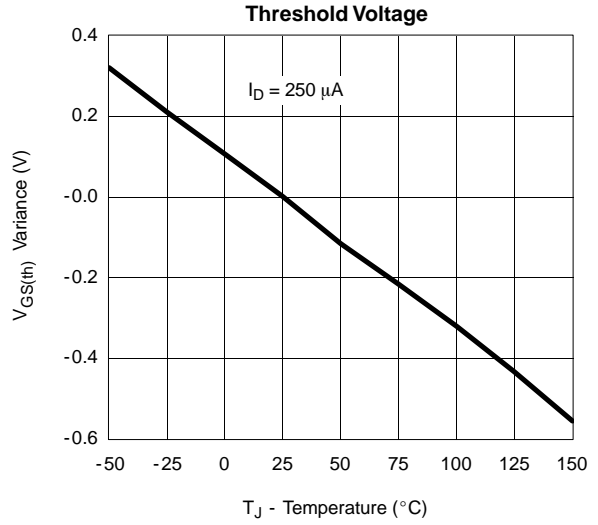
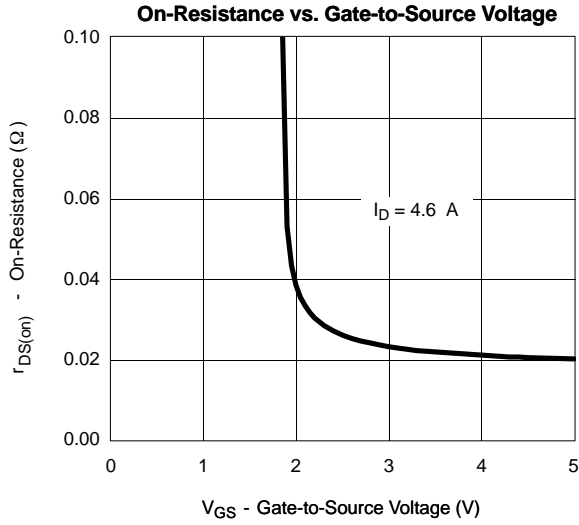


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